ABSTRACT

A system and method for providing a clock signal and data signal delay match to improve setup and hold times for integrated circuits is disclosed. In a simplified embodiment, the system comprises a clock receiver capable of removing noise from a received clock signal. A clock buffer is connected to the clock receiver and is capable of driving the received clock signal to a register. A data receiver is located within the system which is capable of removing noise from received data. In addition at least one miniature clock buffer is located within the system, wherein the at least one miniaturized clock buffer is a scaled version of the clock buffer having a scaling factor of K, the scaling factor representing a number of miniature clock buffers utilized to minimize negative variations experienced by the clock buffer.